

# Altera DSP Development Kit, Stratix V Edition

## 1. Overview



The DSP Development Kit, Stratix<sup>®</sup> V Edition provides a complete design environment that includes all the hardware and software you need to begin developing **DSP-intensive** FPGA designs immediately. The development kit is RoHS compliant. You can use this development kit to do the following:

- Develop and test PCI Express<sup>®</sup> (PCIe<sup>®</sup>) designs at data rates up to Gen3 using the PCIe short card form factor-compliant development board
- Develop and test memory subsystems for DDR3 or QDR II memories
- Use the high-speed mezzanine card (HSMC) connectors to interface to one of over 35 different HSMCs provided by Altera partners, supporting protocols such as Serial RapidIO<sup>®</sup>, 10-Gbps Ethernet, SONET, CPRI, OBSAI, and others

## 2. Specification

### Featured device:

- Stratix V GS FPGA: 5SGSMD5K2F40C2N

### Configuration, status, and setup elements

- JTAG
- **Company: Terasic**
- **Tel: +886-3-5750880**
- **Fax: +886-3-5726690**
- **Add: 9F., No.176, Sec.2, Gongdao 5th Rd, East Dist, Hsinchu City, 30070. Taiwan**

- On-board USB-Blaster™ II cable
- Fast passive parallel (FPP) configuration via MAX® V device and flash memory
- One reset config push button
- One CPU reset push button
- Two configuration push buttons

### **Clocks**

- 50-MHz and 125-MHz programmable oscillators
- SMA input (LVPECL)

### **General user input and output**

- 10/100/1000Mbps Ethernet PHY (SGMII) with RJ-45 (copper) connector
- 16x2 character LCD
- One 8-position dual in-line package (DIP) switch
- Sixteen user LEDs
- Three user push buttons

### **Memory devices**

- DDR3 SDRAM (1,152 MB, x72-bit wide)
- QDR II+ SRAM (4.5 MB, 2-Mb x18-bit wide)
  - Footprint compatible to QDR II 4-Mb x18-bit wide
- RLD RAM II (72-Mbyte CIO RLD RAM II with an 18-bit data bus)

### **Component and interfaces**

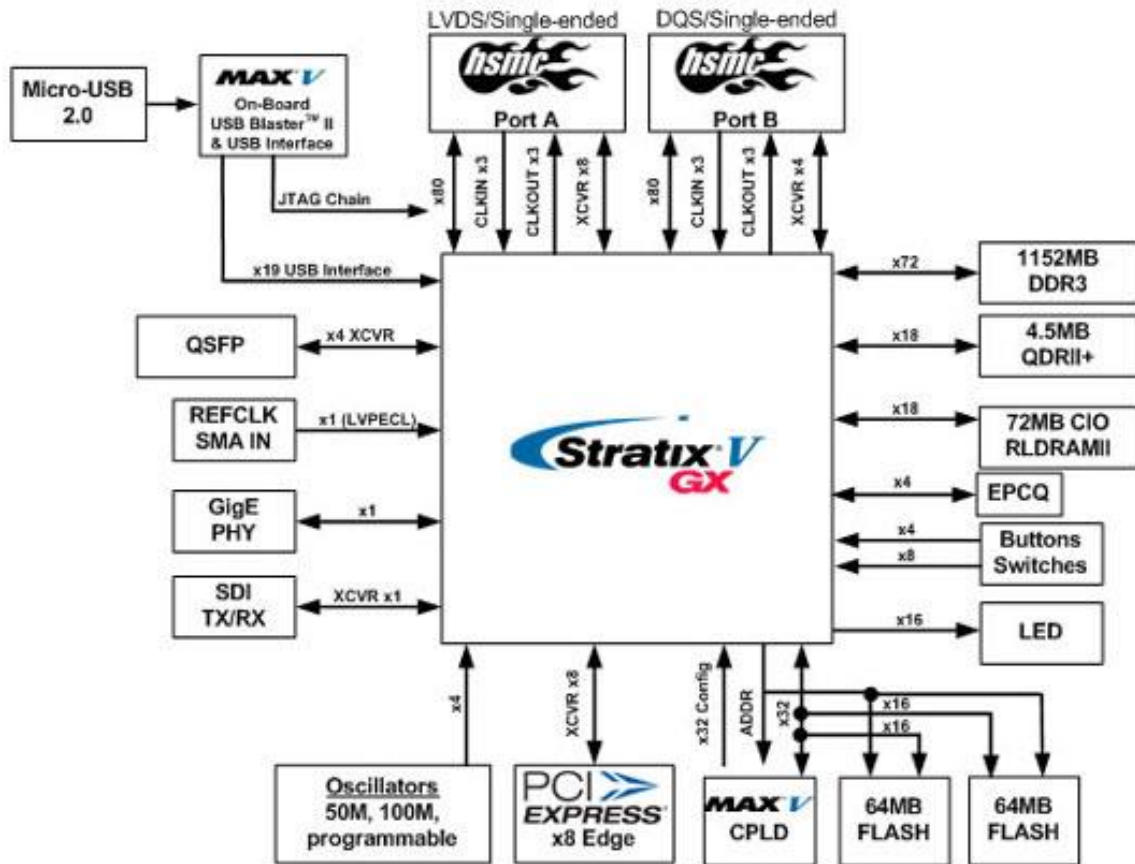
- PCIe x8 edge connector
- Two HSMC connectors
- SMB for serial digital interface (SDI) input and output
- QSFP optical cage
- 10/100/1000Mbps Ethernet PHY (SGMII) with RJ-45 (copper) connector

### **Power**

- Laptop DC input
- PCIe edge connector
- Nios® II processor web server and remote system update

### **Stratix V GX FPGA Development Board Block Diagram**

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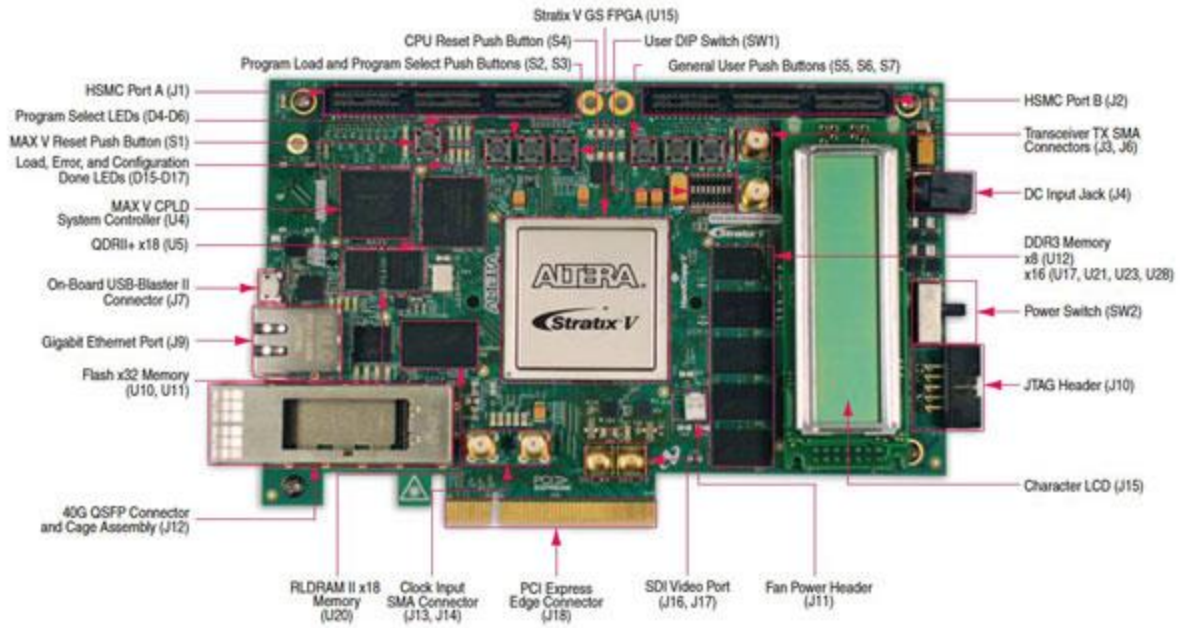


### 3. Kit content

- Loopback and debug HSMC cards
- Power adapter and cables
- Complete documentation
  - User guide
  - Reference manual
  - Board schematics and layout design files
- GUI-based Board Test System
  - Includes complete Quartus II software projects with open source RTL
- Board Update Portal
  - Includes complete Quartus II software projects with open source RTL
- Quartus II design software, Development Kit Edition (DKE)
  - License to use full version of Quartus II software for one year

### 4. Layout

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